A Power PHEMT Device Technology for Broadband Wireless Access

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Abstract **– An unmatched power InGaAs PHEMT transistor in a ceramic package has been developed for broadband wireless access (BWA) applications. Operating at 3.5 GHz, from 12V supplies, a typical device delivers more than 40dBm of peak envelope power at –30 dBc IMD with drain efficiencies as high as 58% in class AB mode. Under the stringent W-CDMA spec of –40 dBc adjacent channel power (with 11.2 dB peak-to-average signal ratio), a small signal gain of 9.5 dB and linear power in excess of 31.5 dBm with 36% efficiency is obtained in class AB mode. Our paper presents the device technology, and the DC and RF performance under W-CDMA and two-tone excitation.**

I. Introduction

As the need for high-speed, high-capacity voice, data, Internet and video services increases, carrier frequencies must increase in order to supply the bandwidth needed for these services. As a result, carrier frequencies have increased into areas where GaAs technologies have historically dominated. To meet the challenge of higher frequency operation, Motorola has developed a pseudomorphic High Electron Mobility Transistor (PHEMT) device technology for BWA infrastructure applications in the S-band frequency range.

II. Device Technology

The Motorola pHEMT device technology, called PH2-HV to distinguish the high voltage version, utilizes a robust 0.6 μm gate length titanium tungsten nitride (TiWNi) gate metallization process to deliver both high manufacturing yield and long term stability under high power operation. The epitaxial structure is a double delta-doped InGaAs/AlGaAs structure grown by molecular beam epitaxy having nominal sheet charge and mobility of $2x10^{12}$ cm^{-2} and 6300 cm^2/Vs at room temperature. The 150 mm (6 inch) wafer process also includes state-of-the-art nickel germanium gold (NiGeAu) ohmic contacts and thick-plated gold interconnects. Highly stable silicon nitride passivation is used to protect the active regions from degradation due to moisture and other atmospheric impurities. A photograph of the passivated FET is shown in Figure 1.

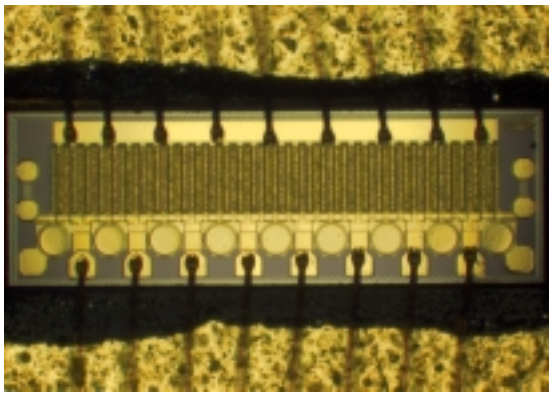

Figure 1. Photograph of a 10W PH2-HV discrete die.

Severe operating conditions encountered in base station applications requires that the FET have good thermal and RF grounding. Thus, the PH2-HV device technology utilizes both a thin GaAs substrate with thick backmetal process, as well as through substrate vias for low source inductance. After front side passivation and 100% DC characterization, the 150 mm wafer is thinned to 25 micron thickness using standard grind and etch techniques, followed by source via etch using reactive ion etching and final backside metallization. Backside metal thickness of 18 micron gold is used to provide good thermal spreading and mechanical stability. A more thorough discussion of the device technology is presented in [1].

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III. DC Device Characteristics

Current-voltage characteristics of a 200 µm FET were measured on a HP4156 semiconductor parameter analyzer. In Figure 2, the drain current versus drain-source voltage (Id-Vds) is shown for gate voltages varying from 0V to –1.0V (-0.2V steps). The Idss current is 215 mA/mm, the threshold voltage is –1.0 Volt and the on resistance (Ron) is 2.4 Ω–mm. The drain current and transconductance versus gate-source voltage (Id,Gm-Vgs) are shown in

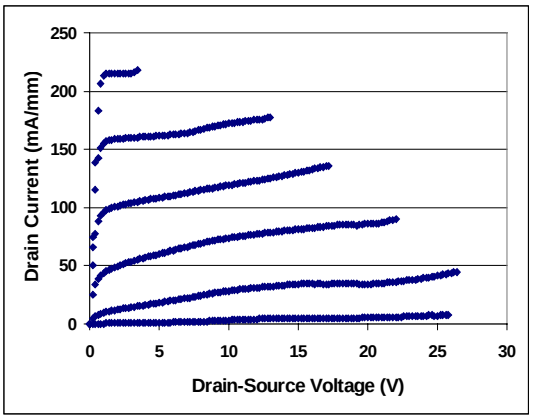

Figure 2. Drain current versus drain source voltage of a 200 µm PH2-HV device.

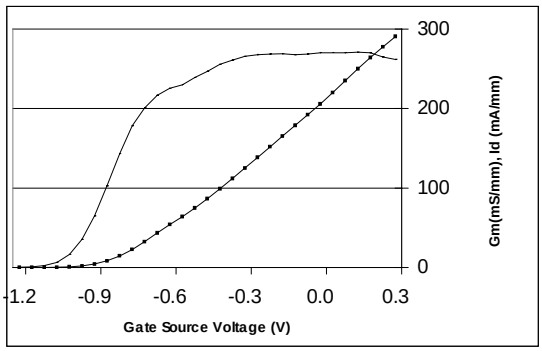

Figure 3. Transconductance and drain current versus gate source voltage for a 200 µm device.

Figure 3. The peak transconductance is 270 mS/mm at Vgs=0V. The larger 15.4 mm FET parameters representative of the PH2-HV device technology are summarized in Table 1. The automated DC test data is obtained on wafer prior to wafer thinning and provides both engineering (statistical) data as well as pass/fail data. The Idmax (Idss) current is measured at Vgs = 0.7 (0V) and at Vds = 1.5V. The lower Idss in the large device compared with the smaller device is most likely due to heating, since the wafer under test is not yet thinned.

Parameter	Typ. Value
Idmax	360 mA/mm
Idss	190 mA/mm
Ron	3.0 Ω-mm
Vth	-1.0 V
BVgd (1mA/mm)	28 V

Table 1. Large FET parameters

IV. Power Performance

The PH2A-HV process has been used to develop a discrete transistor suitable for use as a driver stage in a base station amplifier. A die with 15.4 mm total gate width (see Figure 1) has been chosen for its ability to produce in excess of 10 Watts at 1 dB gain compression, 3.5 GHz and a drain voltage of 12 Volts. The device is packaged in a non-hermetic , bolt-down ceramic package using a 80/20 AuSn eutectic die attach process. A non-hermetic package is utilized for cost savings. The use of a non-hermetic package has been validated by performing a highly accelerated stress and temperature (HAST) test on bare die under normal operating voltages. This test was performed per JEDEC standard JESD22A110B [2]. A photograph of this commercially available transistor is shown in Figure 4.

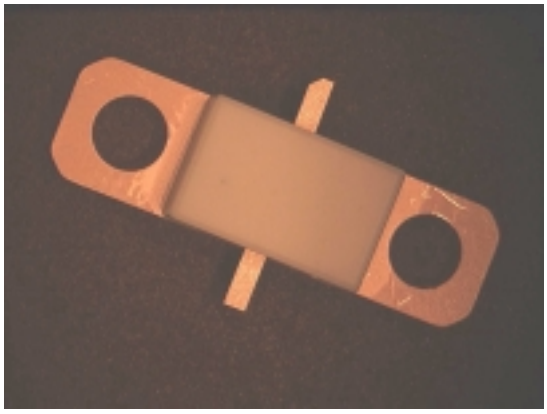

Figure 4. A 10 Watt discrete PHEMT transistor in a bolt down non-hermetic package.

An automated load pull system was utilized to obtain W-CDMA and two tone intermodulation power measurements at a carrier frequency of 3.5 GHz under optimum loading conditions. Forward link W-CDMA with Perch = +50 DPCH and chip

rate = 4.096 MCPS was utilized. This form of W-CDMA modulation has an 11.2 dB peak-to-average at 0.01% probability as defined by the complementary cumulative probability distribution function. Two-tone measurements were made with a 100 kHz carrier spacing.

A "break apart" test fixture was used for all power measurements. The test fixture circuit was fabricated on 20 mil thick microstrip circuit board with 1 ounce copper cladding on both sides. Both the input and output circuit boards were bolted to solid copper blocks to aid in heat dissipation from the device under test (DUT). The DUT is mounted to a copper insert and bolted between each fixture half. One quarter wavelength high impedance microstrip lines were used to supply the DC voltage to the gate and drain terminals. An open circuit stub was utilized on the ¼ wave line to assimilate an open circuit at the fundamental frequency while supplying a near short circuit at the second harmonic frequency.

Load pull testing was accomplished by performing a source pull on the input of the DUT at a class AB amplifier bias voltage. The device was operated at drain-source voltages of 12 Volts. Gate voltages were applied until the proper drain current was reached. An optimum drain current was selected that gave the best all around performance in terms of output power, gain and drain efficiency. Contours of constant transducer power gain, Gt, and input return loss, IRL, were used to select a source impedance state whereby load pull contours could then be generated.

A load pull test was performed at the output of the DUT, in order to generate contours of constant ACP (IMD), output power, and power added efficiency (PAE). A final output impedance state was selected by making a trade-off of the ACP (IMD) and PAE. The input power was swept from low power levels to approximately 2 dB into gain compression.

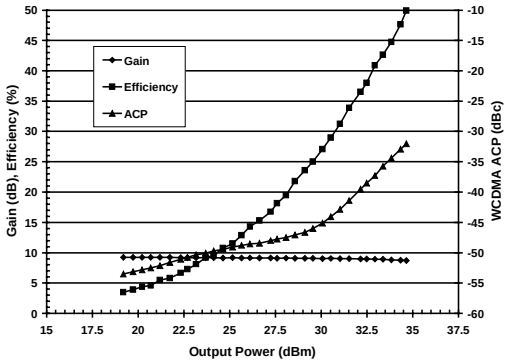

Figure 5. Power gain, drain efficiency and W-CDMA ACP versus output power for a packaged 10 Watt discrete PHEMT transistor. Vds=12 Volts, Ids=180 mA and f=3.5 GHz.

Figure 5 illustrates the power gain, drain efficiency and W-CDMA ACP versus output power for Vds=12 Volts and Ids=180 mA for the packaged device. This is a typical class AB bias. Re-plotting the data as ACP versus drain efficiency, reveals exceptional performance of the packaged device. This can be seen in Figure 6. For an ACP value of –40 dBc the drain efficiency is approximately 36%. As was noted earlier, this data is referenced to the device package leads. Finally, Figure 7 illustrates the packaged device performance under two tone excitation (f_1=3.5 GHz, f_2=3.5001 GHz) for Vds=12 Volts, and Ids=180 mA. These results compare favorably with those presented for competing technologies such as SiC [3].

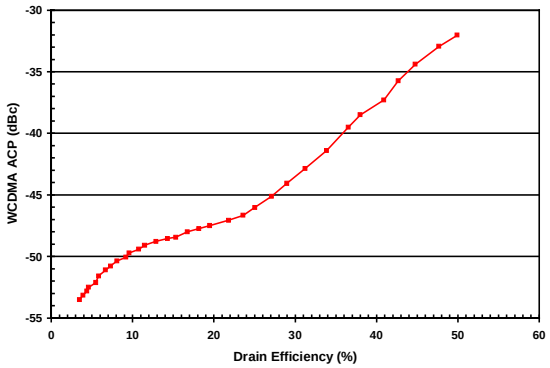

Figure 6. W-CDMA ACP versus drain efficiency for a packaged 10 Watt discrete PHEMT transistor. Vds=12 Volts, Ids=180 mA and f=3.5 GHz.

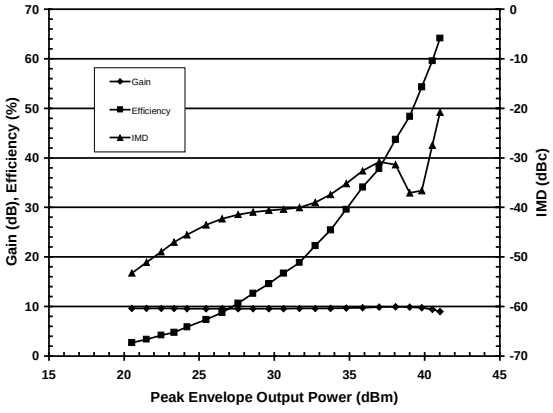

Figure 7. Power gain, drain efficiency and IMD versus peak envelope output power for a packaged 10 Watt discrete PHEMT transister. Vds=12 Volts, Ids=180 mA and f=3.5 GHz.

V. Conclusion

Motorola has developed a PHEMT process designed for BWA applications with 12 Volt operation at carrier frequencies as high as 3.5 GHz. The device fabrication includes plated source vias and 25 μm substrate thickness with 18 μm of back side metal for reduced source inductance and optimum thermal performance.

At 3.5 GHz, under W-CDMA modulation, the packaged device had a power gain of 9.5 dB and drain efficiency of 36% at an ACP of –40 dBc for a class AB bias. The drain efficiency was 58% for a two-tone IMD of –30 dBc. These results represent state-of-the-art power amplifier performance designed for highly linear base station applications at 3.5 GHz.

VI. References

1. W. Peatman, O. Hartin, B. Knappenberger, M. Miller, and R. Hooper, “Power Amplifiers for 3.5 GHz W-CDMA Applications,” 2000 IEEE GaAs IC Symposium, Seattle, WA.
2. “Highly-Accelerated Temperature and Humidity Stress Test (HAST),”JEDEC Solid State Technology Association, JESD22-A110-B, February 1999.
3. S.T. Allen, W.L. Pribble, R.A. Sadler, T.S. Alcorn, Z. Ring, and J.W. Palmour, “Progress in High Power SiC Microwave MESFETs,” 1999 IEEE MTT-S Int’l Microwave Symposium, Anaheim, CA.